

Fig. 2.

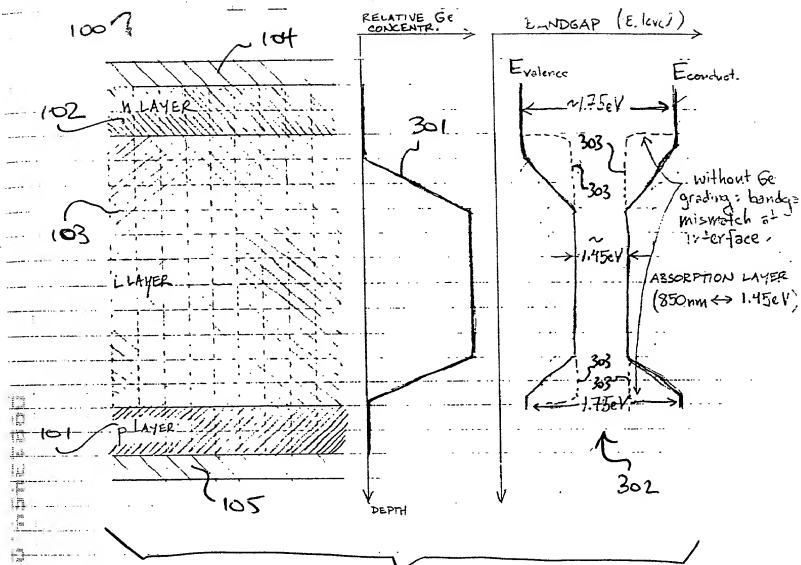


Fig.3

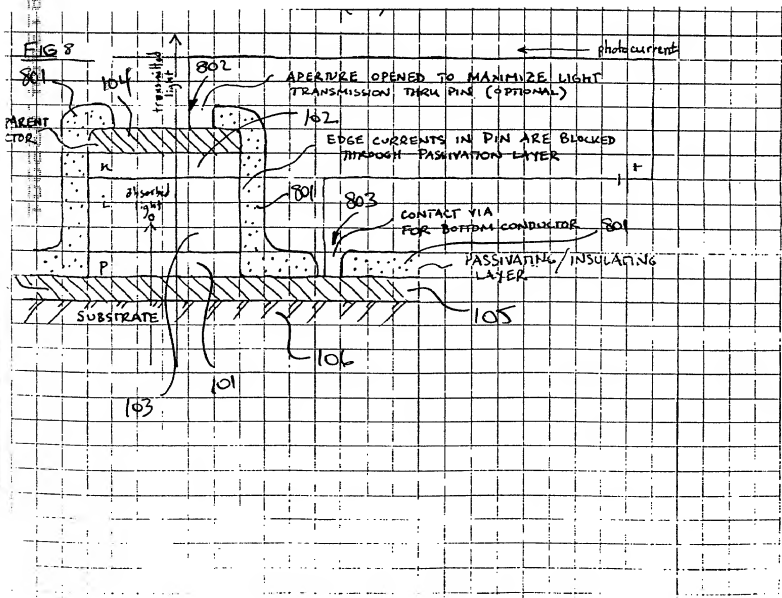
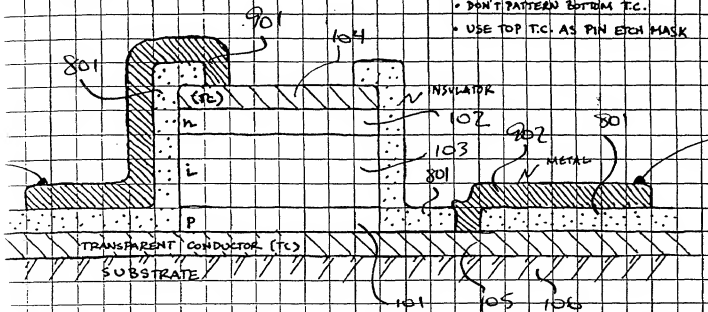


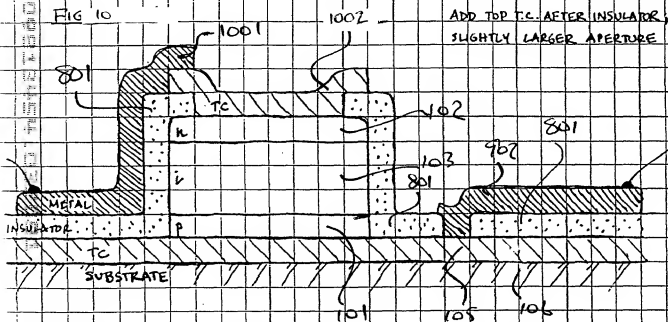
FIG 9



MOST SIMPLE STRUCTURE

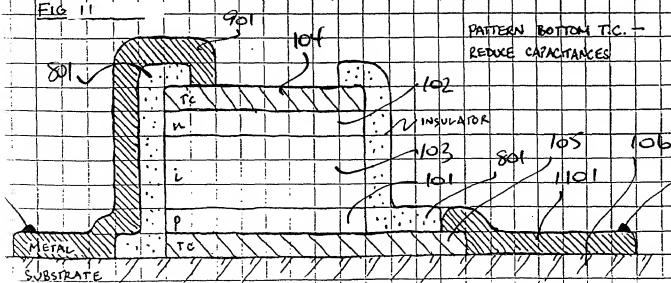
- DON'T PATTERN BOTTOM T.C.
- USE TOP T.C. AS PIN ETCH MASK

FIG 10

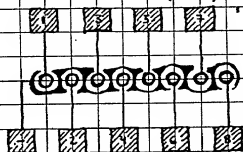
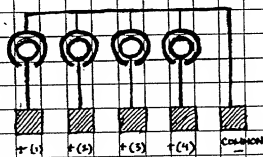
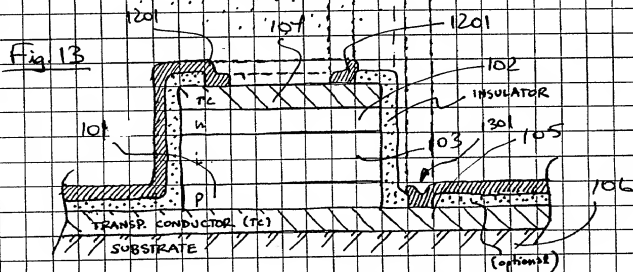
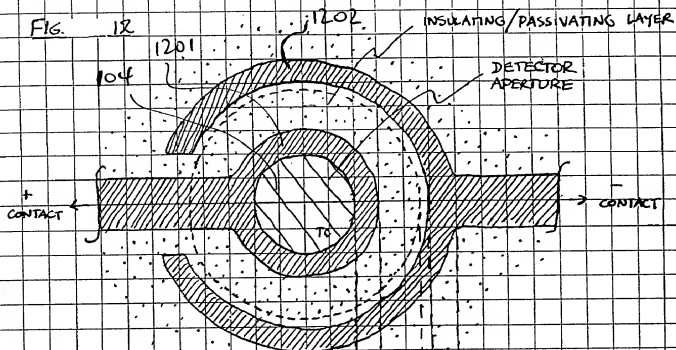


ADD TOP T.C. AFTER INSULATOR
SLIGHTLY LARGER APERTURE

FIG 11



PATTERN BOTTOM T.C. —
REDUCE CAPACITANCES



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Fig. 16

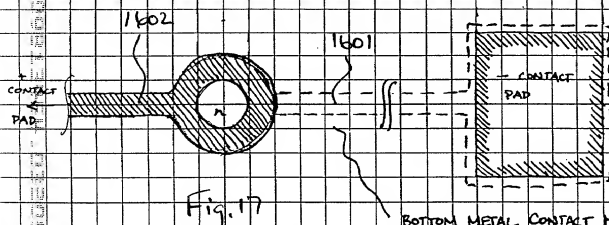
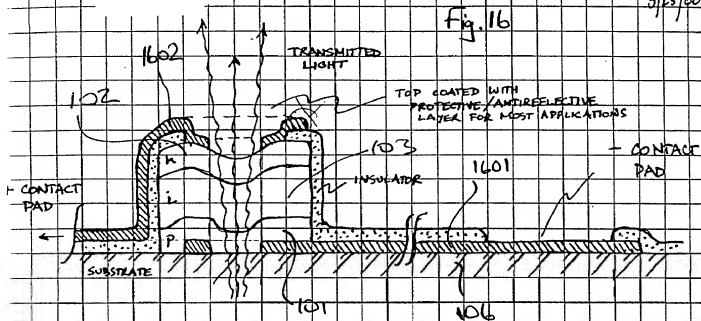


Fig. 17

BOTTOM METAL CONTACT MAY BE USED TO TIE TOGETHER ENTIRE ARRAY

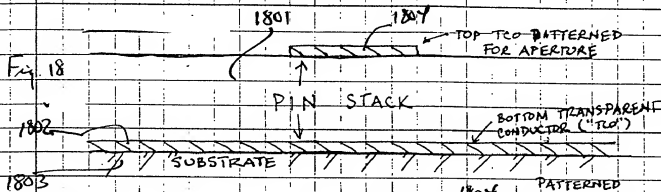


Fig. 19

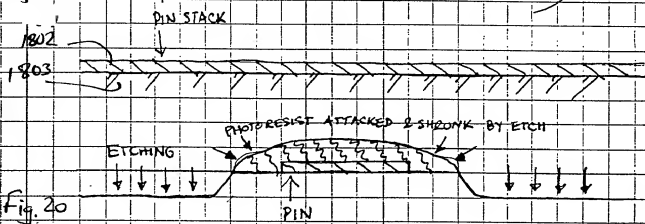


Fig. 21

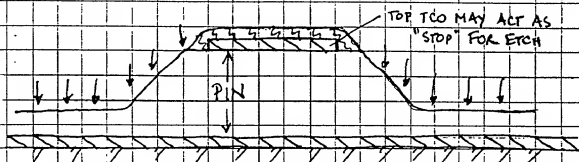
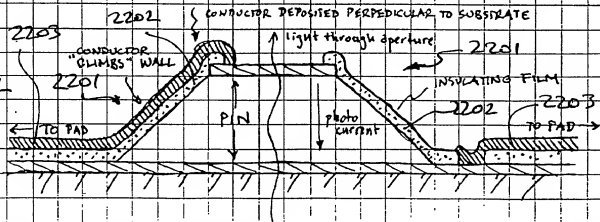


Fig. 22



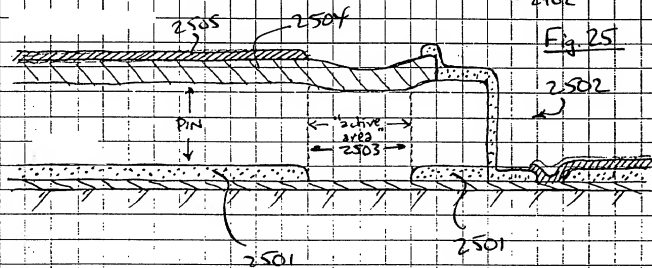
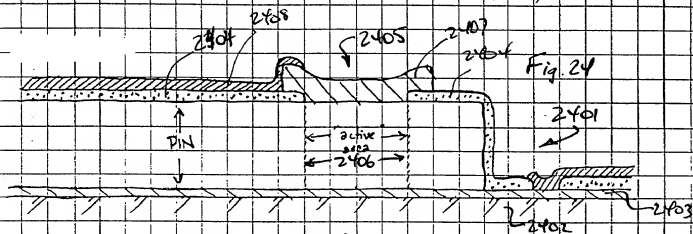
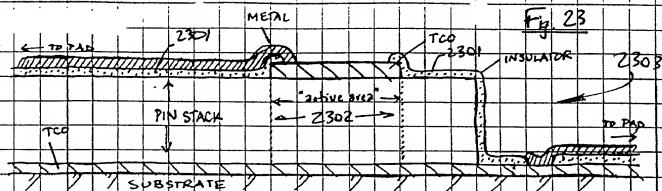


Fig 24

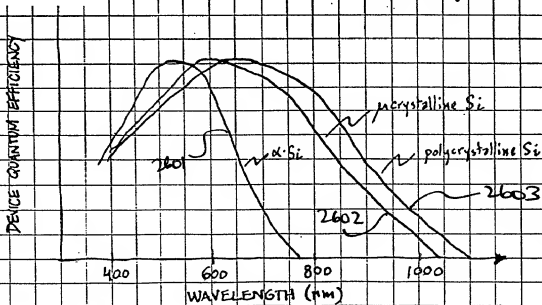


Fig. 27

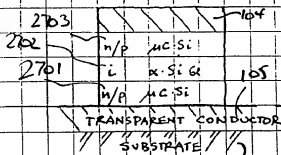


Fig. 28

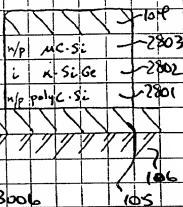


Fig. 29

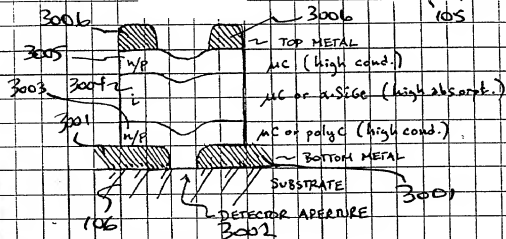
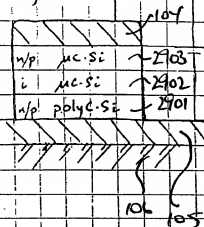


Fig. 30

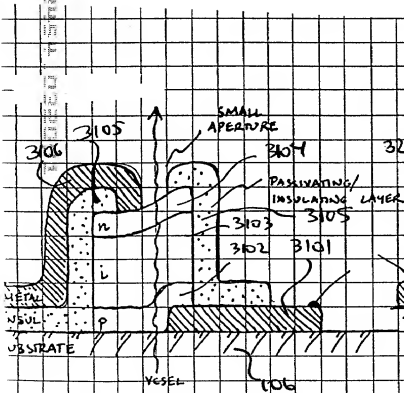


Fig 31

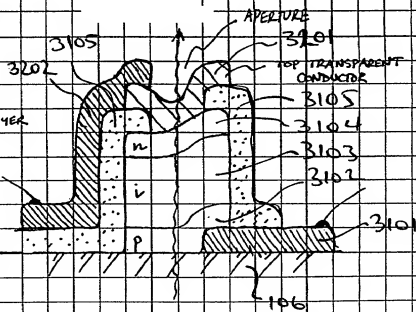


Fig 32

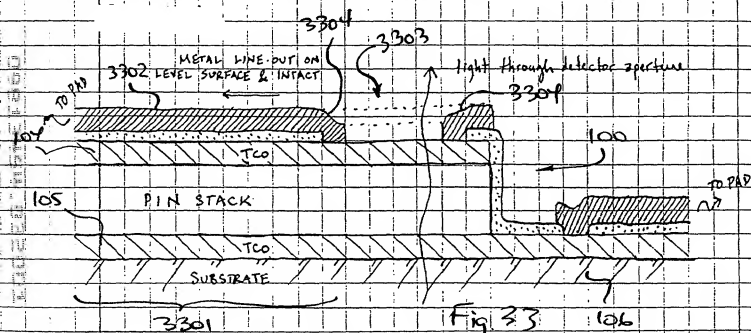
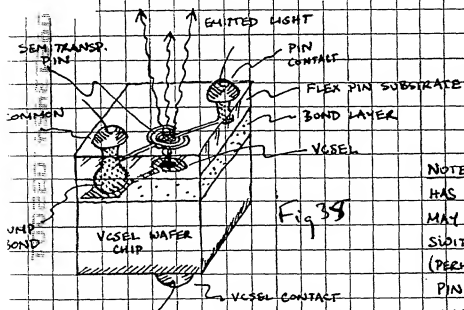
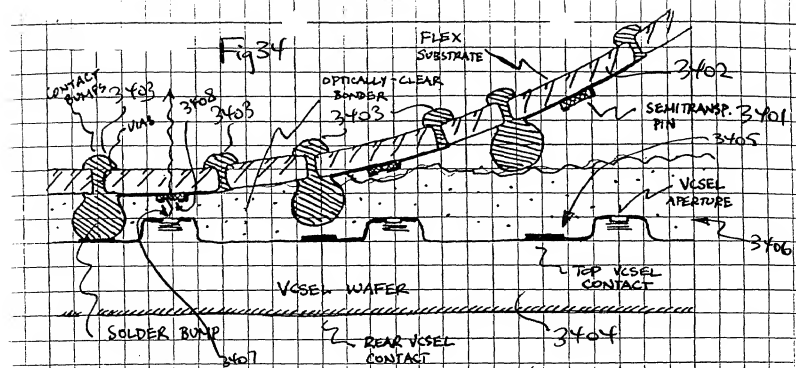


Fig. 33

Fig 34



NOTE: ALTERNATIVE CONFIGURATION HAS 3 TOP CONTACTS (NO COMMON); MAY BE PREFERABLE FOR HIGH-SPD. SWITCHING. (PERHAPS EVEN FORM HOLE THROUGH PIN SUBSTRATE & BOND LAYER TO VCSEL TOP CONTACT).

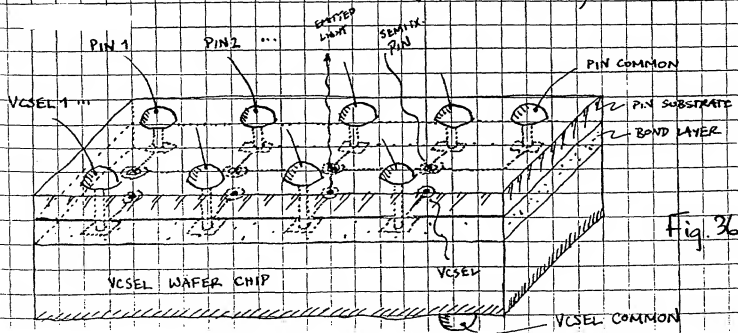


Fig. 36

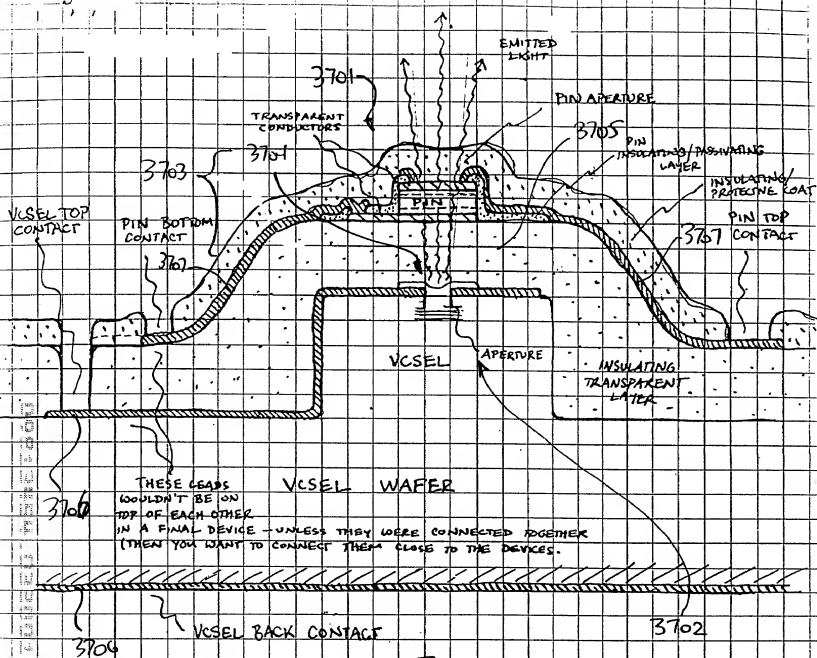


Fig. 37

3/28/00

COLLAPSE LAYERS TO PROVIDE SHORTEST
VCSEL \rightarrow FIBER PATH (NO OPTICS!)

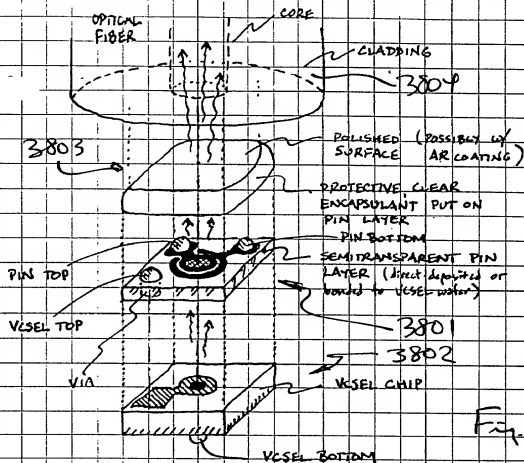


Fig. 38

" SUCH A PACKAGE WOULD ALLOW LOW-COST, DIRECT COUPLING
IN A FIBER CONNECTOR (VCSEL APERTURE $< 25 \mu\text{m}$ AND MULTIMODE
FIBER CORE $\approx 50-62.5 \mu\text{m}$; VCSEL BEAM DIVERGENCE $\leq 20^\circ$, AND
PIN LAYER IS THIN).

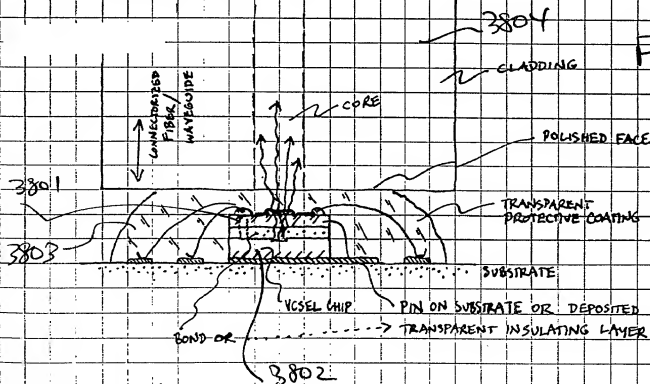
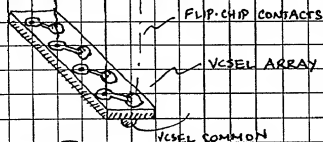
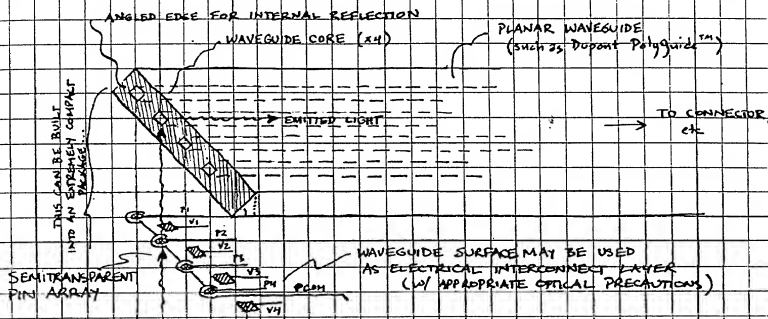


Fig. 39

Fig. 40



PIN ARRAY IS:

- (1) PATTERNED ON WAVEGP.
- (2) PATTERNED ON VCSEL CHIP
- OR (3) PATTERNED ON SEPARATE SUBSTRATE

Fig. 41

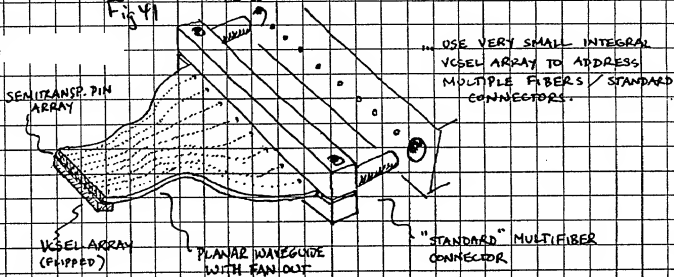


Fig. 42

